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10/805,106	03/19/2004	Mariano G. Fernandez	P19207	8494

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EXAMINER	
NGUYEN, PHILLIP H	

ART UNIT	PAPER NUMBER
2191	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/805,106	FERNANDEZ ET AL.	
	Examiner	Art Unit	
	Phillip H. Nguyen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed 2/1/2008.

2. Claims 1-36 are pending and have been considered below.

Response to Amendment

3. Per applicant's request, claim 36 is newly added.

Response to Arguments

4. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1-36 are rejected under 35 U.S.C. 102(b) as being anticipated by Tsushima et al. (United States Patent No.: 6,044,450).

As per claims 1, 13, and 24:

Tsushima teaches:

accessing a program comprising a plurality of instructions including at least one no operation (NOP) instruction (see at least col. 9:54-55 "**series of instructions (1) – (38) shown in FIG. 9 are executed by the processor**"); and

determining one instruction in the program preceding a determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed (see at least **FIGS. 9-10 - "LD instructions"**; see also col. 10:14-16 "**the first to fourth instructions shown in FIG. 9 are executed by the first to sixth VLIW instructions shown in FIG. 10**"; see also at least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**..."); and

replacing the determined NOP instruction with the determined instruction preceding the determined NOP instruction (see at least **FIG. 11**; see also col. 10:26-27 "**the succeeding NOP instructions are deleted to thereby obtain the VLIW instruction shown in FIG. 11**").

As per claims 2, 14, and 25:

Tsushima further teaches:

deleting one NOP instruction in the program that is not needed to provide a processing delay to ensure that data is available to at least one dependent instruction without moving a non-NOP instruction (see at least **FIG. 11**; see also

col. 10:26-27 "**the succeeding NOP instructions are deleted to thereby obtain the VLIW instruction shown in FIG. 11**").

As per claims 3, 15, and 26:

Tsushima further teaches:

deleting at least one NOP instruction in the program that is not needed to provide the processing delay to ensure the data is available to at least one dependent instruction (see at least **FIG. 11**; see also col. 10:26-27 "**the succeeding NOP instructions are deleted to thereby obtain the VLIW instruction shown in FIG. 11**"); and

after deleting the at least one instruction, replacing at least one NOP instruction with one determined instruction preceding the at least one NOP instruction, whose movement forward to replace the determined NOP instruction will not result in data not being available when needed (see at least **FIG. 11**; see also col. 10:26-27 "**the succeeding NOP instructions are deleted to thereby obtain the VLIW instruction shown in FIG. 11**").

As per claims 4, 16, and 27:

Tsushima further teaches:

performing an additional iteration of deleting at least one instruction and then replacing the at least one NOP instruction in response to replacing at least one NOP instruction (see at least **FIGS. 9-11**).

As per claims 5, 17, and 28:

Tsushima further teaches:

wherein the instructions in the program comprise assembly language instructions coded by a developer (see at least **FIG. 9**; see also col. 9:3-5 "**It is assumed that a program shown in FIG. 9 is obtained by coding this benchmark program by the assembler language**...").

As per claims 6, 18, and 29:

Tsushima further teaches:

determining whether the accessed NOP instruction is needed to delay processing of one dependent instruction following the accessed NOP instruction to ensure that data is available to the dependent instruction accessing the data (see at least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**..."); and

deleting the accessed NOP instruction in response to determining that the NOP instruction is not needed to ensure that data is available to the dependent instruction accessing the data (see at least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**...").

As per claims 7, 19, and 30:

Tsushima further teaches:

identifying instructions preceding the NOP instruction that have a delay in writing the results (see at least FIG. 9; see also col. 9:9-15 "**LD of the first to fourth instructions represents a load instruction. With his load instruction, data in the main storage at an address (an address designated by a (K+10)th element of an array Z or by a variable T, R or Q) designated by the second operand of this instruction is loaded into a register (the 26th, 1st, 2nd or 3rd floating point register FR 26...**"; see also col. 9:61-65 "**executes the load instruction and that the number of machine cycles (latency) is "2" which is required for the calculation results to become usable**..."); and

identifying dependent instructions following the NOP instruction that are dependent on an availability of data from the identified instructions having the delay in writing the results (see at least FIG. 9; see also col. 9:17-21 "**MOVE of the fifth instruction is a data move instruction. With this data move instruction, the contents of the register (the 26th floating point register FR26) represented by the second operand are copied to the register (the 4th floating point register FR24) represented by the first operand**").

As per claims 8, 20, and 31:

Tsushima further teaches:

wherein the determining of one instruction in the program to move forward comprises determining one instruction whose movement forward to replace the determined NOP instruction will not result in data not being available to one dependent instruction following the NOP instruction (see at least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**...").

As per claims 9, 21, and 32:

Tsushima further teaches:

wherein the one previous instruction comprises a preceding instruction closest to the accessed NOP instruction in the program (see at least **FIG. 9 - LD instruction**).

As per claims 10, 22, and 33:

Tsushima further teaches:

deleting at least one NOP instruction not needed to ensure that data accessed by the dependent instruction is available to the dependent instruction, wherein the operations of replacing accessed NOP instructions with previous non-NOP instructions are performed after deleting NOP instructions not needed to ensure that data accessed by the dependent instruction is available (see at

least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**...").

As per claims 11, 23, and 34:

Tsushima further teaches:

wherein the determined instruction is further not a branch target instruction (see at least **FIG. 9** - load instruction).

As per claims 12, 24, and 35:

Tsushima further teaches:

wherein the program instructions are for execution by an engine in a multiprocessor engine (see at least **FIG. 1**).

As per claim 36:

Tsushima further teaches:

wherein determining one instruction in the program preceding the determined NOP instruction whose movement forward to replace the determined NOP instruction will not result in data not being available when needed comprises determining whether the instruction to move forward causes the data needed by one dependent instruction to be written in fewer cycles such that the

number of cycles between a writing instruction and the dependent instruction are not sufficient to guarantee that the written data will be available to the dependent instruction (see at least **FIGS. 9-10 -"LD instructions"**; see also col. 10:14-16 "**the first to fourth instructions shown in FIG. 9 are executed by the first to sixth VLIW instructions shown in FIG. 10**"; see also at least col. 10: 35-45 "**the NOP number sub-field is assumed as having a 3 bit length. Therefore, the number of succeeding NOP instructions, only 0 to 7, can be set to one NOP number sub field, and all these succeeding NOP instructions can be deleted**...").

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip H. Nguyen whose telephone number is (571) 270-1070. The examiner can normally be reached on Monday - Thursday 10:00 AM - 3:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Y. Zhen can be reached on (571) 272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PN
3/27/2008

/Wei Zhen/

Supervisory Patent Examiner, Art Unit 2191